DESCRIPTION

2-STAGE A/D CONVERTER AND IMAGE SENSOR USING THE SAME

TECHNICAL FIELD

The present invention relates to the improvement of an A/D converter, and an image sensor using the same.

BACKGROUND ART

One major characteristic of a CMOS image sensor is that various functional circuits can be integrated on the image sensor, and one such functional circuit to be integrated is an A/D converter circuit. By this, a digital output image sensor can be integrated and the system can be compact, and also the influence of noise that enters the output of the sensor chip can be eliminated.

An A/D converter to be integrated on an image sensor is disclosed in the following documents.

[1] A. Simoni, A. Sartori, M. Gottaidi, A. Zorat: "A digital vision sensor", Sensors and Actuators, A46 - 47, pp. 439 - 443, 1995

[2] B. Mansoorian, H. Y. Yee, S. Huang, E. Fossum: "A 250 mW 60 frames/s 1280x 720 pixel 9b CMOS digital image sensor". Dig. Tech. Papers, Int. Solid-State Circuits

Conf., pp. 312- 313, 1999

[3] T. Sugiki, S. Ohsawa, H. Miura, M. Sasaki, N. Nakamura, I. Ioune, M. Hoshino, Y. Tomizawa, T. Arakawa: "A 60 mW 10b CMOS imaging sensor with column-to-column FPN reduction", Dig. Tech. Papers, Int. Solid-State Circuits Conf., pp. 108 - 109, 2000

[4] S. Decker, R. D. McGrath, K. Bremer, C. G. Sodini: "A 256 x 256 CMOS image array with wide dynamic range pixels and column-parallel digital output", IEEE J. Solid-State Circuits, Vol. 33, No. 12, Dec. 1998

[5] Japanese Patent Application Laid-Open No. 2002-232291

The above-mentioned "A digital vision sensor" discloses a technology for integrating 8-bit integral type A/D converter elements using a lamp signal generator, comparator and register in columns. A similar technology is also disclosed in "DESCRIPTION" of patent No. 2532374.

The above-mentioned "A 60 mW 10b CMOS imaging sensor with column-to-column FPN reduction" also discloses a technology for integrating the integral type A/D converter elements in columns, and 10-bit elements are implemented using a comparator of which accuracy has been improved. For these integral type A/D converters, it is difficult to implement a higher resolution since the conversion time is long, and particularly increasing

resolution makes the conversion time longer exponentially. However linearity is superb.

The above-mentioned "A 250 mW 60 frames/s 1280x 720 pixel 9b CMOS digital image sensor" discloses a technology for arranging successive approximation type A/D converters using a capacitor in columns so as to operate, which is appropriate for image sensors with a high frame rate and many pixels, since high-speed A/D conversion is possible. However the actual precision still remains around 8 bits.

The above-mentioned "A 256 x 256 CMOS image array with wide dynamic range pixels and column-parallel digital output" discloses a technology for arranging the cyclic A/D converter elements in columns so as to operate, which is also suitable for high-speed A/D conversion. However the resolution is about 9 bits.

The above-mentioned Japanese Patent Application Laid-Open No. 2002-2322915 discloses a technology for performing 2-stage integral type A/D conversion on signals of which noise is cancelled in columns, but this is not for improving the signal noise ratio (SNR) by 2-stage conversion, since the amplification function is not included.

In addition to the above, a few image sensors having A/D conversion elements within the pixel have been reported, but are omitted here since they are not

directly related to the present invention.

DISCLOSURE OF THE INVENTION

Conventional A/D converters for an image sensor use only the advantage of arranging the A/D converters in columns so as to operate in parallel.

The present invention provides an A/D converter for an image sensor, which performs a part of the A/D conversion functions by using a noise cancellation circuit in columns, and performs amplification simultaneously with this, thereby obtaining a high signal noise ratio (SNR) and implementing an A/D converter with a high resolution along with the A/D conversion sections in a subsequent stage, and each can implement a digital image sensor with high sensitivity and wide dynamic range.

It is an object of the present invention to perform A/D conversion with maintaining high resolution and high SNR in an image sensor by performing N-bit A/D conversion along with noise cancellation operation in columns, and performing M-bit A/D conversion in columns or after performing horizontal scanning on residual analog values.

It is another object of the present invention to simplify circuits by having an amplifier that cancels noise perform a part of the A/D conversion.

The present invention is applied to an image sensor, for example, but is not limited to this application.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram depicting a 2-stage A/D converter for performing A/D conversion on the analog residual after horizontally scanning;

Fig. 2 is a block diagram depicting a 2-stage A/D converter for performing A/D conversion on the analog residual in columns;

Fig. 3 is a diagram depicting a unit circuit for performing column amplification and N-bit A/D conversion (A/D conversion first);

Fig. 4 is a diagram depicting a unit circuit for performing column amplification and N-bit A/D conversion (pull-back method);

Fig. 5 is a diagram depicting a circuit example of 4 times amplification and 2-bit A/D conversion;

Fig. 6 is a diagram depicting a 4-transistor pixel circuit;

Fig. 7 is a timing chart depicting a 2-bit column A/D conversion operation;

Fig. 8 is a table showing the change of ϕA, ϕB, ϕC and ϕD with respect to the value D in 2-bit A/D conversion;

Fig. 9 is a diagram depicting a column read circuit for performing pull-back type N-bit A/D conversion and

generating analog residuals;

Fig. 10 is a diagram depicting an example of a circuit which performs noise cancellation and pull-back while performing 8 times amplification;

Fig. 11 is a diagram depicting the operation of the pull-back A/D conversion;

Fig. 12 is a diagram depicting the relationship between the input and output of an amplifier;

Fig. 13 is a diagram depicting a circuit for performing noise cancellation, 2 times amplification and 1-bit A/D conversion;

Fig. 14 is a diagram depicting the transmission characteristics of the circuit in Fig. 13; and

Fig. 15 is a diagram depicting a variant form of the circuit in Fig. 9, which outputs the amplifier reset level and the analog residual output separately.

BEST MODE FOR CARRYING OUT THE INVENTION

Fig. 1 is a block diagram depicting the first embodiment. The element circuits (1), which perform signal amplification and N-bit A/D conversion arranged in an array in the columns of the image sensor, are operated in parallel. The analog residual thereof is horizontally scanned, and M-bit A/D conversion (2) is performed on the output thereof, so as to perform N + M-bit A/D conversion.

The control lines S, TX and R, from the vertical

shift register, correspond to each control line in Fig. 6.

Fig. 2 is a block diagram depicting the second embodiment. Here the element circuits (1), for performing noise cancellation, signal amplification and N-bit A/D conversion arranged in an array in the columns of the image sensor, perform A/D conversion in parallel, and M-bit A/D conversion elements, arranged in an array, are operated on the analog residual output.

Fig. 3 and Fig. 4 show the configuration of the unit circuits (1) which perform noise cancellation, amplification and N-bit A/D conversion in columns. In any case, in the columns of the image sensor, N-bit A/D conversion is performed while performing amplification with G times gain, and a predetermined value is subtracted according to the result, so that a saturation of the output of the amplifier is prevented. In Fig. 3, N-bit A/D conversion is performed first on the pixel output, and the predetermined value is subtracted from the pixel output signal so that the output of the amplifier enters a linear operation range.

In the case of Fig. 4, G times of amplification is performed first on the pixel output, A/D conversion is performed on this amplified output, D/A conversion is performed on this result, a predetermined value is subtracted from the input of the amplifier, and this process is repeated until the output of the amplifier

enters a linear range. This is called the "pull-back method".

Various configuration to perform an equivalent operation as above are possible, and the configuration of the present invention is not limited strictly to this block diagram. In Fig. 3 and Fig. 4, a function to cancel the noise generated in the pixel section is not clearly shown, but the noise cancellation function can be integrated into the amplification function by the G times amplifier. An actual example of this will be described later.

Fig. 5 shows a circuit diagram in the case of 2-bit A/D conversion, which corresponds to the configuration in Fig. 3. Fig. 6 shows the configuration example of the pixel section. This is a pixel circuit of 4 transistors + 1 photo-diode, using a buried photo-diode. Another circuit, such as a 3-transistor pixel circuit, may be used instead.

The photoelectric charges converted by the buried photo-diode (PD) are fetched by transistors (MIN, MX), and are output to the output ends of the pixel group via a signal line. This signal is applied to the A/D converter (2-bit ADC) as the pixel output, and is connected to the input of the amplifier (3) having gain G via the capacitor 4C (having 4 times the capacitance compared with capacitor C). From the A/D converter (4),

the control signals ϕA, ϕB, ϕC and ϕD, corresponding to the level of the input signal, are output.

The A/D conversion value by the A/D converter is D/A converted by the switch which is controlled by the control signals ϕA, ϕB, ϕC and ϕD, and the D/A converter (5) based on the capacitors C and 2C (note: 2C has double the capacity of C), and this result is subtracted from the input. In other words, the output Y with respect to the input X is determined as follows

[Expression a1]

$$Y = G \times X - R \times D \quad (a1)$$

Here R is a full scale (FS) value of the input. For G, G = 4 is normally used in the case of 2 bits, but a greater value may be used to provide a larger amplification function.

D is a result of the A/D conversion at 2 bits, and is determined as follows.

[Expression a2]

$$D = \begin{cases} 0\ (X \le FS/4) \\ 1\ (FS/4 < X \le FS/2) \\ 2\ (FS/2 < X \le 3FS/4) \\ 3\ (3FS/4 < X \le FS) \end{cases} \quad \text{(a2)}$$

This D is output as the higher 2-bit A/D conversion value. Y, on the other hand, is an analog residual output value.

Fig. 7 shows a timing chart when the above operation is performed by combining the pixel circuits in Fig. 5 and Fig. 6. From the pixel output (sensor output), the reset level V_R and the signal level V_s are output, as shown in Fig. 7.

$\phi 1$, $\phi 2$, $\phi 3$ and $\phi 4$ are the control signals for switching the switch circuit near the amplifier.

First the input and the output of the amplifier are shorted with $\phi 1 = 1$, and the level of V_R is sampled into the capacitor 4C. At this time $\phi 2 = 1$. Then by setting $\phi 1 = 0$, $\phi 2 = 0$ and $\phi 3 = 1$, the level of V_s is provided to 4C. As a result, a signal when $V_R - V_s$ is amplified 4 times appears in the output of the amplifier. Also $X = V_R - V_s$ is provided to the 2-bit A/D converter, and ϕA ϕB, ϕC

and ϕD change according to the result. As a consequence, the output voltage (analog residual output) is determined according to Expressions (a1) and (a2) as $R = V_{R2} - V_{R1}$. When the comparator in the 2-bit A/D converter is sampling, $\phi A = \phi C = 1$ and $\phi B = \phi D = 0$. At the timing when this comparison result is output, ϕA, ϕB, ϕC and ϕD are changed, as shown in Fig. 8.

Fig. 9 shows a circuit for performing pull-back A/D conversion in the columns and calculating the analog residual, and Fig. 10 shows a concrete circuit example of the input section thereof. Fig. 11 shows the operation timing chart thereof. The pixel circuit is assumed to be a 4-transistor type which transfers charges within the pixel, as shown in Fig. 6. Other pixel circuits, such as a 3-transistor pixel circuit, can be used in the same manner by changing the timing. First the reset level V_k is output, then the signal level V_s is output.

Fig. 11 shows the case of 8 times amplification. First the input and the output of the amplifier is shorted with $\phi 1 = 1$, $\phi 2 = 1$ and $\phi 3 = 0$, and one end of the feedback capacitor is connected to Vref, and the V_R level is sampled into the capacitor 8C having 8 times the capacitance compared with the capacitor C. Then after setting to $\phi 1 = 0$, $\phi 2 = 0$ and $\phi 3 = 1$, the signal level V_s is supplied to 8C. As a result, a signal of $V_R - V_s$,

amplified to 8 times, appears in the output of the amplifier. If $V_R - V_s$ is large, however, the applied signal exceeds the linear range of the amplifier, and is saturated. However if the charge Q_0 in the input section of the amplifier is not changed at this time, the output of the amplifier can be pulled back into a linear range by using the capacitor in the input section.

When V_R is being sampled, the charge Q_0 in the input section of the amplifier is given by the following expression.

[Expression 1]

$$Q_0 = 8C(V_0 * - V_R) + C(V_0 * - V_{REF}) + 4C(V_0 * - V_{SW0}) + C_i V_0 *$$

(1)

Here V_0* is the voltage of the amplifier input section when V_R is being supplied, and C1 is the parasitic capacitance between the amplifier input unit and the ground point. V_{SW0} is the initial voltage of the stair case waveform.

After the input is switched to V_s and the feedback capacitance C is connected to the amplifier output, the following expression is established if Q_0 is not changed.

[Expression 2]

$$Q_0 = 8C(V_0 - V_S) + C(V_0 - V_{OUT}) + 4C(V_0 - V_{SW}) + C_i V_0$$

(2)

Here V_{SW} is the voltage of the staircase waveforms.

And V_0 is the voltage of the amplifier input section when V_s is being sampled. If $V_R - V_s$ is large at this time, the amplifier is saturated, and V_0 largely changes from V_0*. However if V_{SW} is operated and pulled back to the area where the amplifier operates at high gain, then the following expression is established.

[Expression 3]

$$V_{OUT} = A(V_0^* - V_0) + V_0^* \quad (3)$$

Here A is an open loop gain of the amplifier. If A is sufficiently large, V_0* - V_0 must be roughly zero to receive voltage with which V_{out} operates in a linear area, since this circuit is operating as a negative feedback circuit. This can be understood easily if it is considered in the same manner as the case when a negative feedback circuit is constructed using an operation amplifier of which the open loop gain is large, where the differential voltage of the plus input and the minus input for operation is roughly zero.

Now if (1) and (2) are regarded as simultaneous equations where V_0* - V_0 = 0, then the following expression can be acquired.

[Expression 4]

$$V_{OUT} = V_{REF} + 8(V_R - V_S) - 4(V_{SW} - V_{SW0})$$

(4)

This means that the output voltage becomes a voltage when V_R - V_s amplified 8 times is added to V_{REF}, then 4 times the differential voltage of V_{SW} - V_{SW0} is subtracted from the result. In other words, by operating the amplifier so that Q_0 does not change and pulling back the amplifier to the point where the amplifier operates at high gain, the linear operation determined by Expression (4) can be performed.

With this approach, a circuit which performs A/D conversion using a staircase waveform generator and a comparator and which generates a residual analog value can be constructed as shown in Fig. 9. As the timing chart in Fig. 11 shows, the output of the staircase waveform generator remains as V_{SW0} initially, and when amplification is performed, the output of the amplifier is saturated, and is clipped. Then if the staircase waveform is supplied, the output of the amplifier enters an area where the amplifier operates at high gain at a certain point, and Expression (4) is satisfied, then the output of the amplifier decreases according to the level of the staircase waveform. So if the comparator performs comparison operation (sampling (S) and decision (D)) for the output of the amplifier and the threshold value V_T

each time a step of the staircase waveform rises, the output of the comparator changes from High to Low at a point when the output of the amplifier becomes V_T or less. By this, the sample and hold circuit (S/H) connected to the output of the amplifier samples and stores the signal at this point. This becomes the analog residual. The number of steps when the output of the amplifier becomes V_T or less at this time becomes the A/D conversion value. There are 5 steps in the case of Fig. 11.

If one step of the staircase waveform is ΔV_S, Expression (4) can be written as follows, where the number of steps is D.

[Expression 5]

$$V_{OUT} - V_{REF} = 8(V_R - V_S) - 4D\Delta V_S \quad (5)$$

Fig. 12 is a diagram depicting this relationship when $V_T = 4\Delta V_S$. In order to store the value D, which corresponds to the A/D conversion value, a code corresponding to the number of steps of the staircase waveform (e.g. graycode, binary code is also acceptable) is supplied to the data latch, and the code is stored in the data latch by the output of the comparator. In Fig. 12, when 3-bit A/D conversion is possible and the input of the analog residual of the amplifier output is in a 0

to V_T range, the output thereof also comes in a 0 to V_T range.

There are many advantages to performing this processing in the initial stage on the columns of the image sensor. First as Expression (5) shows, the difference of the reset level and the signal level of the pixel section is amplified while performing the above function, fixed pattern noise generated and reset noise in the pixel section can be cancelled, and the 1/f noise generated in the pixel section can also be decreased.

Also amplification can be performed at high gain while preventing the saturation of the output of the amplifier. This can dramatically decrease the influence of noise which is applied on the circuit thereafter, and an image sensor with low noise level can be implemented. Also by partially performing A/D conversion by this circuit, the A/D conversion circuit, to be connected in a subsequent stage, can be simplified, and the burden on this A/D conversion circuit can be decreased.

Finally, this processing is particularly advantageous when an integral type A/D conversion is used in a subsequent stage of the above mentioned circuit. An integral type A/D converter is widely used as a high precision A/D conversion system since it is superb in linearity, but the problem thereof is that the conversion time is long. An integral type A/D converter supplies

the lamp signal and the input signal to the comparator, and the count of the clock until the lamp signal exceeds the input signal, counted by the counter, is used as the A/D conversion value, and if 10-bit A/D conversion is performed by an integral type, counting up to 1024 is normally required. A technology to perform 10-bit A/D conversion using an integral type on the image sensor has been reported, but it is difficult to apply this to a high-speed image sensor.

If 3-bit A/D conversion is performed in advance and integral type A/D conversion is performed on the analog residual, as in the present invention, then the count can be 1/8, that is 128, and the integral type can be used for a high-speed image sensor. In the case when A/D conversion is performed with very high resolution, and 10-bit and 1024 counts can be implemented as the integral type A/D conversion, 3-bit A/D conversion is performed beforehand, then an A/D conversion equivalent to 13 bits can be performed, and an image sensor with high resolution digital output can be implemented.

The analog residual in Fig. 12 is ideally in a 0V to V_T range, but if an error occurs to the decision of the comparator, the analog residual exceeds this range. So the analog input range of the A/D conversion in a subsequent stage on the analog residual is set to wider than this range. Then even if a minor error occurs to

the comparator, this does not influence the final A/D converted digital value, and the accuracy requirements of the comparator can be relaxed.

Fig. 12 is the case of 3 bits and 8 times amplification, and the voltage range of the analog residual output can be increased by choosing the gain to be 2^N when N-bit A/D conversion is performed. If the resolution of the A/D conversion is high however, gain becomes very high and implementation may become difficult. In this case, the gain may be set to lower than 2^N. In such a case, the analog residual output becomes small, but the gain of the S/H circuit may be set to a value higher than 1, as shown in Fig. 9 (G_2 in the case of Fig. 9), for amplification.

Fig. 13 shows the third embodiment. This is a configuration when 1-bit A/D conversion is performed while performing noise cancellation and two times amplification in columns. This circuit can be applied to a pixel circuit where the signal level is output first, and the reset level is output later.

When the amplifier output is V_{OUT}, the signal level of the output of the pixel section is V_s, the reset level is V_R, and the differential voltage thereof is $\Delta V_{in} = V_R - V_s$, the following expression is established.

[Expression 6]

$$V_{out} = -2\Delta V_{in} + V_{R1} - D(V_{R1} - V_{R2})$$

(6)

Here D is an A/D conversion value, and is defined as follows.

[Expression 7]

$$D = \begin{cases} 0\ (V_S > V_T) \\ 1\ (V_S \leq V_T) \end{cases}$$

(7)

In other words, this circuit changes the reference bias voltage of the amplifier output depending on the result of A/D conversion. An example is given. When the signal level V_s changes in a 2V to 1V range and V_R is 2V, it is assumed that VT = 1.5V. At this time, ΔV_{in} changes in a 0 - 1V range. If V_{R1} = 2V, V_{R2} = 3V in Expression (6) at this time, then V_{OUT} changes as shown in Fig. 14 with respect to ΔV_{in}.

While the change range of the input signal is 1V, the output can also be confined in a 1V range from 2V to 1V. The gain of the output, with respect to the input signal, is 2 times. In this way the amplification range of the output can be confined to 1V, even if the input

signal level is doubled to increase sensitivity.

Fig. 15 shows a circuit where a sample & hold circuit, for storing the reset level of the amplifier, is installed to remove the offset voltage of the column amplifier. The pixel circuit used here is a 4-transistor type, which transfers charges within the pixel, as shown in Fig. 6. Other pixel circuits, such as a 3-transistor pixel circuit, can be used in the same manner by changing the timing. It is assumed that the reset level V_R is output first, then the signal level V_s is output.

First the input and the output of the amplifier are shorted with $\phi 1 = 1$ and $\phi 2 = 1$, and the V_R level is sampled into 8C. Then the output of the amplifier is stored in one sample & hold circuit with $\phi 1 = 0$ and $\phi 2 = 0$. Then TX in the pixel is opened so as to supply the signal level V_s to 8C. As a result, a signal of $V_R - V_s$ amplified to 8 times appears in the output of the amplifier. In this case, when V_R is being sampled, the charge Q_0 in the input section of the amplifier is given by the following expression.

[Expression b1]

$$Q_0 = 8C(V_0 * - V_R) + 4C(V_0 * - V_{SW0}) + C_i V_0 *$$

(b1)

If Q_0 does not change after the input is switched to V_s and the feedback capacitance C is connected to the

amplifier output, the following expression is established.

[Expression b2]

$$Q_0 = 8C(V_0 - V_S) + C(V_0 - V_{OUT}) + 4C(V_0 - V_{SW}) + C_i V_0$$

(b2)

Here V_{SW} is the voltage of the staircase waveform. If $V_R - V_s$ is large at this time, the amplifier saturates and V_0 dramatically changes from V_0*. However if V_{SW} is operated and the amplifier is pulled back to the area where the amplifier operates at high gain, then V_0* - V_0 approaches zero by negative feedback.

Now if (b1) and (b2) are regarded as simultaneous equations where V_0* - V_0 = 0, then the following expression can be acquired.

[Expression b3]

$$V_{OUT} = V_0^* + 8(V_R - V_S) - 4(V_{SW} - V_{SW0})$$

(b3)

This means that the output voltage becomes a voltage when $V_R - V_s$ amplified 8 times is added to V_0*, then 4 times the differential voltage of $V_{SW} - V_{SW0}$ is subtracted from the result. If the output V_0* when the amplifier is shorted is sampled and held, and the difference from the output of another sample & hold circuit storing the result of Expression (b3) is determined, and the offset voltage of the amplifier is cancelled.

With the exception of this point, the rest of the operation is the same as Fig. 9. $\phi 3$ in Fig. 15 is controlled by the output of the comparator, just like the case of the sample & hold circuit in Fig. 9.

INDUSTRIAL APPLICABILITY

According to the configuration described above, the analog residual, after the first A/D conversion with N bits, is amplified, and the second A/D conversion with M bits is performed on this result, therefore M-bit A/D conversion can be performed with high resolution, about 10 bits, so if the N-bit A/D conversion in the first stage is 3 bits or 4 bits, then an A/D conversion with extremely high resolution, such as 13 bits - 14 bits, is possible, and a digital output image sensor with a wide dynamic range can be implemented.

Also as an A/D converter for an image sensor, if a part of the A/D conversion functions is performed by a noise cancellation circuit in columns and amplification is performed simultaneously, then A/D conversion with high resolution can be implemented along with the A/D conversion section in a subsequent stage, while increasing the high signal noise ratio (SNR).